What is claimed is:

1. An apparatus for producing digital output signals from an analog input signal in a pipelined converter, the apparatus comprising:

a sample-and-hold amplifier (SHA) circuit that includes an SHA input terminal that is coupled to the analog input signal and an SHA output terminal, wherein the SHA circuit is arranged to provide a sampled voltage (V_{SHA}) that is responsive to the analog input signal;

an evaluator circuit that includes an evaluation input terminal that is coupled to the analog input signal (V_{IN}) and a digital output terminal that is arranged to provide digital codes that are responsive to the analog input signal;

a reference circuit that includes an adjustment input terminal that is coupled to the digital output terminal, and a reference output terminal, wherein the reference circuit is arranged to provide a reference voltage (V_{REF}) that is responsive to at least one of the digital codes; and

a multiplying digital-to-analog converter (MDAC) circuit that includes an MDAC input terminal that is coupled to the SHA output terminal, an MDAC output terminal that is arranged to provide an output voltage (V_{OUT1}), and a reference input terminal (V_{REFMD}) that is arranged receive the reference voltage (V_{REF}), wherein the MDAC circuit is arranged to sample the reference voltage (V_{REF}) and the sampled voltage (V_{SHA}) at substantially the same time such that the reference voltage is pre-sampled in the pipelined converter.

2. The apparatus of claim 1, the sample-and-hold amplifier (SHA) circuit comprising a sampling circuit and a sampler block that is arranged to cooperate with a gain block.

3. The apparatus of claim 1, the sample-and-hold amplifier (SHA) circuit comprising a sampling capacitor circuit, a feedback capacitor circuit, and an amplifier circuit, wherein the sampling capacitor is arranged to sample the analog input signal

during a first operating phase, and wherein the sampling capacitor, the feedback capacitor, and the amplifier circuit are arranged to provide the sampled voltage (V_{SHA}) during a second operating phase, wherein the sampled voltage (V_{SHA}) is related to the analog input signal (V_{IN}) by a gain factor.

4. The apparatus of claim 3, the sample-and-hold amplifier (SHA) wherein the sampling capacitor circuit, the feedback capacitor circuit, and the amplifier circuit are arranged to cooperate with one another such that: the sampling capacitor circuit is coupled to the analog input signal during the first operating phase, the feedback capacitor is initialized during the first operating phase, the sampling capacitor is decoupled from the analog input signal during the second operating phase, and the amplifier is arranged to redistribute the charges between the sampling capacitor and the feedback capacitor during the second operating phase.

5. The apparatus of claim 2, wherein the gain block has a gain of 1.

6. The apparatus of claim 1, wherein the evaluator circuit comprises a flash-type converter.

7. The apparatus of claim 1, wherein the evaluator circuit comprises a 1.5-bit sub-ADC.

8. The apparatus of claim 1, wherein the evaluator circuit comprises a sampling capacitor, a comparator circuit, and a digital logic circuit that are arranged to cooperate with one another such that: the sampling capacitor samples the analog input signal during a first operating phase to provide a sampled signal, the comparator circuit evaluates the sampled signal after the first operating phase to provide at least one evaluation signal, and the digital logic circuit provides the digital code in response to the at least one evaluation signal.

9. The apparatus of claim 1, wherein the evaluator circuit comprises a sampling capacitor, a first comparator circuit, a second comparator circuit, and a digital logic circuit that are arranged to cooperate with one another such that: the sampling capacitor samples the analog input signal during a first operating phase to provide a sampled signal, the first comparator circuit evaluates the sampled signal after the first operating phase to provide at first evaluation signal, the second comparator circuit evaluates the sampled signal after the first operating phase to provide a second evaluation signal, and the digital logic circuit provides the digital code in response to the first and second evaluation signals.

10. The apparatus of claim 9, wherein the first and second comparator circuits are arranged to compare the sampled signal to $+V_{REF}/4$ and $-V_{REF}/4$, respectively.

11. The apparatus of claim 10, wherein the reference circuit further arranged such that: V_{REFMD} corresponds to $-V_{REF}$ when the sampled signal is greater than $+V_{REF}/4$, V_{REFMD} corresponds to $+V_{REF}$ when the sampled signal is less than $-V_{REF}/4$, and V_{REFMD} corresponds to 0V when the sampled signal is between $-V_{REF}/4$ and $+V_{REF}/4$.

12. The apparatus of claim 1, the multiplying digital-to-analog converter (MDAC) circuit comprising: a sampling capacitor circuit (C_S), a feedback capacitor circuit (C_F), and an amplifier circuit are arranged to cooperate with one another such that: the sampling capacitor samples the sampled voltage (V_{SHA}) during a second operating phase, the feedback capacitor samples the MDAC reference voltage (V_{REFMD}) during the second operating phase, and the sampling capacitor, the feedback capacitor, and the amplifier circuit provide the output voltage (V_{OUT1}) during a first operating phase, wherein the sampled voltage (V_{SHA}) is related to the output voltage (V_{OUT1}) according to a transfer function.

13. The apparatus of claim 12, wherein the transfer function comprises:

$$V_{OUT1} = \left(1 + \frac{C_S}{C_F}\right) \cdot V_{SHA} + 1$$, when V_{IN} is evaluated as less than a first predetermined threshold;

$$V_{OUT1} = \left(1 + \frac{C_S}{C_F}\right) \cdot V_{SHA}$$, when V_{IN} is evaluated as greater than a second predetermined threshold; and

$$V_{OUT1} = \left(\frac{C_S}{C_F}\right) \cdot V_{SHA}$$, when V_{IN} is evaluated as between the first and second predetermined thresholds.

14. The apparatus of claim 1, wherein the apparatus is arranged such that the sampled voltage (V_{SHA}) is sampled by the SHA circuit during a first operating phase, the analog input signal (VIN) is evaluated by the evaluator circuit prior to a second operating phase such that the reference circuit selects the reference voltage (V_{REF}) prior to the second operating phase, wherein the MDAC circuit is further arranged to: sample the sampled voltage (V_{SHA}) during the second operating phase, sample the selected reference voltage (V_{REF}) during the second operating phase, and adjust the output voltage during the first operating phase.

15. An apparatus for producing digital output signals from an analog input signal in a pipeline converter, the apparatus comprising:

a sample-and-hold amplifier means that is arranged to provide a sampled voltage (V_{SHA}) that is responsive to the analog input signal (V_{IN});

an evaluator means that is arranged to provide digital codes that are responsive to the analog input signal (V_{IN});

a reference means that is arranged to provide a selected reference voltage (V_{REF}) that is responsive to at least one of the digital codes from the evaluator means; and

a multiplying digital-to-analog converter (MDAC) means that is arranged to sample the selected reference voltage (V_{REF}) and the sampled voltage (V_{SHA}) at

substantially the same time such that the selected reference voltage (V_{REF}) is pre-sampled in the MDAC means, and also arranged to provide an output voltage (V_{OUT1}) that is associated with a residue signal of the pipeline converter.

16. The apparatus of claim 15, wherein the MDAC means comprises a sampling capacitor means and a feedback capacitor means, wherein the sampling capacitor means has a value corresponding to C_S and the feedback capacitor means has a value corresponding to C_F, the transfer curve comprising:

$V_{OUT1} = \left(1 + \frac{C_S}{C_F}\right) \cdot V_{SHA} + 1$, when V_{IN} is evaluated as less than a first predetermined threshold;

$V_{OUT1} = \left(1 + \frac{C_S}{C_F}\right) \cdot V_{SHA}$, when V_{IN} is evaluated as greater than a second predetermined threshold; and

$V_{OUT1} = \left(\frac{C_S}{C_F}\right) \cdot V_{SHA}$, when V_{IN} is evaluated as between the first and second predetermined thresholds.

17. The apparatus of claim 16, wherein the first predetermined threshold corresponds to –VREF/4 and the second predetermined threshold corresponds to +VREF/4.

18. A method for converting an analog input signal to a digital code in the first stage of a pipeline converter, the method comprising:

sampling the analog input signal during (V_{IN}) a first operating phase with a SHA circuit to provide a sampled signal (V_{SHA}) after the first operating phase;

evaluating the analog input signal (V_{IN}) during the first operating phase with an evaluator circuit to provide a digital code after the first operating phase;

selecting a reference voltage (V_{REF}) from a reference circuit in response to the digital code before a second operating phase;

sampling the sampled signal during the second operating phase with a sampling capacitor (C_S) in an MDAC circuit;

sampling the selected reference voltage (V_{REF}) during the second operating phase with a feedback capacitor (C_F) in the MDAC circuit; and

configuring the sampling capacitor, the feedback capacitor, and an amplifier in a feedback loop to adjust an output voltage (V_{OUT1}) during the first operating phase, whereby the selected reference voltage is pre-sampled in the MDAC circuit to provide enhanced DNL performance in the pipeline converter.

19. The method of claim 18, wherein the first operating phase corresponds to a sampling phase, and the second operating phase corresponds to an amplification phase in the pipeline converter.

20. The method of claim 18, wherein a transfer function associated with the output voltage comprises:

$V_{OUT1} = \left(1 + \frac{C_S}{C_F}\right) \cdot V_{SHA} + 1$, when V_{IN} is evaluated as less than a first predetermined threshold;

$V_{OUT1} = \left(1 + \frac{C_S}{C_F}\right) \cdot V_{SHA}$, when V_{IN} is evaluated as greater than a second predetermined threshold; and

$V_{OUT1} = \left(\frac{C_S}{C_F}\right) \cdot V_{SHA}$, when V_{IN} is evaluated as between the first and second predetermined thresholds.